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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/830,963	07/06/2001	Yogo Kawasaki	P280152	5294
22850	7590	07/15/2005	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			PATEL, ISHWARBHAI B	
			ART UNIT	PAPER NUMBER
			2841	

DATE MAILED: 07/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.



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APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
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EXAMINER

ART UNIT	PAPER
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0705

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Commissioner for Patents

Amendment to specification and interview summary attached.


KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

EXAMINER'S AMENDMENT

1. This examiner's amendment is necessitated based on the query before publication.

During prosecution of the application, original claims, claims 1-25, were cancelled. New claims 26 and 27 were added and subsequently the new claims were allowed (notice of allowance mailed on January 27, 2005). However, in the specification, under the heading "Disclosure of the Invention", page 5, line 23 to page 19, line 19, original claim 1-25 were referred to. To avoid the confusion the specification is amended as shown below. No new matter is added.

Authorization for this examiner's amendment was given in a telephone interview with Masayasu Mori (Reg. 47,301) on July 8, 2005.

The application has been amended as follows:

In the specification, delete line 23, page 5 to line 19, page 19 and add:

According to one aspect of the present invention, a multi-layer printed circuit board includes a core substrate having opposite first and second sides, and first and second buildup layers provided on the first and second sides of the core substrate respectively. The first buildup

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layer has first interlayer resin insulating layers and first conductor layers alternately provided. The second buildup layer has second interlayer resin insulating layers and second conductor layers alternately provided. Each of through holes electrically connects the first conductor layers and the second conductor layers at opposite ends of each of the through holes. Each of through hole lands is electrically connected to each of the through holes between the opposite ends of each of the through holes. First via holes are provided right on the ends of the through holes to be electrically connected to the through holes. Second via holes are provided to be electrically connected to the through hole lands.

According to another aspect of the present invention, resin filler is filled in the through holes, and the first and second conductor layers are formed to cover exposed surfaces of the resin filler from the through holes. The first via holes are formed on the conductor layers.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ishwar (I. B.) Patel
Examiner
Art Unit: 2841
July 8, 2005